SCHEME OF INSTRUCTION AND EXAMINATION
B. E. -ECE
Scheme and Syllabus for

Honors in VLSI Design

SNo	Code	Course Title	Scheme of Instruction			Contact Hrs/Wk	Scheme of Evaluation			Credits
			L	T	P		Hrs	CIE	SEE	
Theory										
1	HR501EC	Advanced System Design	3	-	-	**3**	3	40	60	3
2	HR601EC	Fundamentals of System Verilog	3	-	-	**3**	3	40	60	3
3	HR602EC	Design for Testability	3	-	-	3	3	40	60	3
4	HR701EC	Intelligent CAD	3	-	-	**3**	3	40	60	3
5	HR702EC	CMOS Analog and Mixed Signal IC Design	3	-	-	**3**	3	40	60	3
6	HR861EC	Project	-	-	6	**6**	-	-	100	3
		Total	**15**	**-**	**6**	**21**	**15**	**200**	**400**	**18**

Course Code	Course Title						Core/PE/OE
HR501EC	**Advanced System Design**						**Core**
Prerequisite	**Contact Hours Per Week**				CIE	SEE	Credits
	L	T	D	P			
	3	-	-	-	40	60	**3**

Course Objectives

The objectives of this course is

1. To learn the basic philosophy and bus architectures for RISC architectures
2. Know the SoC architectures and features of ARM
3. Learn the instructions for assembly coding of ARM
4. Design SoC solutions for various solutions

Course outcomes

After completing this course, the student will be able to:

1. Understand the basics of RISC architecture philosophy for ARM and SoC
2. Explore the features and architectures of ARM cortex-M4 SoC
3. Write Assembly codes using ARM Cortex M4 for simple Arithmatic and Logic operations
4. Design various Bus Configurations like GPIO, UART, I2C and SPI for STM32F
5. Design real time interfaces such as seven segment displays, LCD, motors etc and use them in various applications

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	1	1	1	1	-	-	-	-	-	-	1
CO2	2	1	2	1	1	-	-	-	-	-	-	1
CO3	3	2	3	2	3	3	-	-	-	2	1	2
CO4	3	2	3	3	3	3	2	1	1	2	1	2
CO5	3	2	3	3	2	3	2	1	1	2	1	2

Correlation rating: Low / Medium / High: 1 / 2 / 3 respectively

UNIT-I:

Introduction to Advanced System Design (ARM Cortex IP): The ARM RISC design philosophy, System hardware – AMBA bus, System software; ARM registers bank, status registers; vector table, data flow model.

UNIT-II:

Cortex M4 SoC Architecture: Cortex M SoC Processor: introduction – Block diagram; Interrupts and Processor Reset Sequence.CortexM4, STM32F features; Memory Map; ARM Bus Matrix; Nested Vectored Interrupt Controller (NVIC), Interrupts Vs Exceptions; Cortex M Processor Modes.

UNIT-III:

ARM Instruction Set Architecture (ARM ISA): Fundamentals of ARM instructions, ARM Assembly instructions: Data processing, Branching, Load-store, SWI and Program Status Register instruction. Thumb ISA.

UNIT-IV:

SoC Programming (STM32F): GPIO Management: Accessibility & Configurations; Timer Programming; UART: Configuration, baud rate generation, UARTx drivers in C; I2C: Features, modes, Pins and Registers; I2C Driver Programming; SPI: master/slave operation, Pins & Registers; ADC Driver for data sampling & processing needs.

UNIT-V:

ARM Interfacing with Real World: Interfacing of switches, LEDs; Seven Segment Display; Matrix Keypad; LCD – Design options; DC Motor & Stepper Motor interfacing designs in Embedded C/C++; debugging methods.

Suggested Reading

1. ARM System-on-chip Architecture by Steve Furber, Pearson Education, ISBN978-81-317-0840-8, 2E, 2012.
2. STM32 ARM Programming for Embedded Systems, Muhammad Ali Mazidi, Shujen Chen, Eshragh Ghaemi ISBN: 978-099-792-5944, 2018
3. Muhammad Tahir and Kashif Javed, "ARM® Microprocessor Systems: Cortex®-M Architecture, Programming, and Interfacing", CRC Press, © 2017 by Taylor & Francis Group, LLC.

Course Code	Course Title						Core/PE/OE
HR601EC	**Fundamentals of System Verilog**						**Core**
Prerequisite	**Contact Hours Per Week**				CIE	SEE	Credits
	L	T	D	P			
-	3	-	-	-	40	60	**3**

Course Objectives: The course is taught with the objectives of enabling the student to:

1. To Know Basics of System Verilog
2. To Familiarize with Object Oriented Programming
3. To Explore Randomization and Threads in System Verilog
4. To Know Test Coverage in System Verilog

Course Objectives : On completion of the course, students will be able to

1. To understand the basic concepts of Design Verification
2. To Construct User Defined Data Types in System Verilog
3. To Create Object Oriented Programming Environment
4. To Create Object Oriented Programming Environment
5. To understand the Coverage Concepts

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	1	1	2	-	-	-	-	-	-	-	-	-
CO2	1	1	2	2	3	-	-	-	-	-	-	1
CO3	1	2	2	2	3	-	-	-	-	-	-	1
CO4	1	2	2	2	3	-	-	-	-	-	-	1
CO5	1	2	2	2	3	-	-	-	-	-	-	1

Correlation rating: Low / Medium / High: 1 / 2 / 3 respectively

UNIT-I:

Verification Guidelines: Introduction, Verilog vs System Verilog, Verification Process , Verification Plan, Verification Methodology Manual, Basic Testbench Functionality, Directed Testing, Testbench Components, Layered Testbench, Building a Layered Testbench, Simulation Environment Phases

UNIT-II:

DATA TYPES: Built-in Data Types, Fixed-Size Arrays, Dynamic Arrays, Queues, Associative Arrays, Linked Lists, Array Methods, choosing a Storage Type, Creating New Types with typedef, Creating User-Defined Structures, Enumerated Types, Constants, Strings, Net Types

Tasks & Functions: Tasks, Functions, and Void Functions, Routine Arguments, Local Data Storage, Time Values, Procedural Statements

UNIT-III:

Basic OOP concepts: Object Oriented Programming significance and advantages, classes, objects, objecthandles, methods, Static and Global Variables, using one class inside another class, Dynamic objects, copying objects, Public Vs Local and Building a test bench. Inheritance, Overriding, Data Hiding and Encapsulation, Abstract Classes and Virtual Methods. Scope Resolution Operator, Classes Extern Methods, type def classes

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UNIT-IV:

Randomization: Randomization in System Verilog, Constraint Details,, Solution Probabilities, Controlling Multiple Constraint Blocks, Valid Constraints, In-line Constraints, The pre_randomize and post randomize Functions, Common Randomization Problems, Iterative and Array Constraints

THREADS AND INTERPROCESS COMMUNICATION: Interprocess Communication, Events, Semaphores, Mailboxes.

UNIT-V:

Coverage: Introduction to Coverage, Coverage Types, Functional Coverage Strategies, Anatomy of a Cover Group, Triggering a Cover Group, Data Sampling, Cross Coverage

Introduction to Universal Verification Methodology (UVM)

Suggested Reading

1	Christ Spear and Greg Tumbush, System Verilog for Verification, 3 rd ed., Springer, 2012
2	Gamma, Erich, Helm, Richard, Johnson, Ralph, and Vissides, John, Design Patterns: Elements of Reusable Object-Oriented Software. Reading, MA: Addison-Wesley 1995
3	Sutherland, Stuart, Davidmann, Simon, and Flake, Peter. SystemVerilog for Design. Norwell, MA: Kluwer Academic Publishers, 2004

Course Code	Course Title						Core/PE/OE
HR602EC	**Design for Testability**						**Core**
Prerequisite	**Contact Hours Per Week**				CIE	SEE	Credits
DSD	L	T	D	P			
	3	-	-	-	40	60	**3**

Course Objectives: The course is taught with the objectives of enabling the student to:

1. To Understand testability fundamentals and fault models
2. To understand the significance of fault simulation
3. To understand test generation for SSFs
4. To learn about scan architectures
5. To understand specific and random BIST.

Course Objectives: On completion of this course, the student will be able to :

1. Understand modeling at various abstraction levels , delay and logic simulation
2. Understand fault classes and their models
3. Understand and apply test generation algorithms for SSFs
4. Understand boundary scan standards
5. Understand BIST architectures

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	2	-	-	-	-	-	-	-	-	-	-	1	-	-
CO2	2	-	-	-	-	-	-	-	1	-	-	1	2	-
CO3	2	2	2	-	-	-	-	-	1	-	-	1	2	-
CO4	2	2	-	-	-	-	-	-	1	-	-	1	2	-
CO5	2	1	-	-	-	-	-	-	-	-	-	1	1	-

Correlation rating: Low / Medium / High: 1 / 2 / 3 respectively

UNIT-I

Introduction to Test and Design for Testability (DFT): Fundamentals. Modeling: Modeling digital circuits at logic level, register level and structural level.

Logic Simulation: Types of simulation, Delay models, Element evaluation, Hazard detection, Gate level event driven simulation

UNIT-II

Fault Modeling – Logic fault models, Fault detection and redundancy, Fault equivalence and fault location. Single stuck and multiple stuck – Fault models. Fault simulation applications, General techniques for Combinational circuits

Unit -III

Test Generation algorithms for SSFs: Combinational Circuits-Fault oriented ATG- algorithms and selection criteria, fault independent ATG, ATG for sequential circuits using iterative array model.

UNIT-IV

Design for testability – testability trade-offs, techniques. Scan architectures and testing – controllability and absorbability, generic boundary scan, full integrated scan, storage cells for scan design. Board level and system level DFT approaches. Boundary scan standards.

UNIT-V

Built In Self-Test (BIST): BIST concepts, Specific BIST architectures – CSBL, BILBO, Random logic BIST-BIST process- Pattern generation – Response compaction , Circuit initialization, Test point insertion.

Suggested Reading

1. Miron Abramovici, Melvin A. Breur, Arthur D. Friedman, Digital Systems Testing and Testable Design, Jaico Publishing House, 2001
2. M.L. Bushnell and V.D. Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwer Academic Publishers, 2002
3. Robert J. Feugate, Jr., Steven M. Mentyn, Introduction to VLSI Testing, Prentice Hall, Englehood Cliffs, 1998
4. Parag. K. Lala, "Fault tolerant and fault testable hardware design",BS Publications, 2002

Course Code	Course Title						Core/PE/OE
HR701EC	**INTELLIGENT CAD**						**Core**
Prerequisite	**Contact Hours Per Week**				CIE	SEE	Credits
	L	T	D	P			
-	3	-	-	-	40	60	**3**

Course Objectives: The course is taught with the objectives of enabling the student to:

1. To provide an in-depth understanding of VLSI design automation tools, algorithms, system design, structural and logic design.
2. To equip students with knowledge and skills in VLSI design automation, including floor planning and routing concepts, placement algorithms, gate-level and switch-level modeling and simulation.
3. To provide comprehensive knowledge in combinational logic synthesis, ROBDD principles, two-level logic synthesis, and both gate-level and switch-level modeling and simulation.
4. To explore advances and challenges in applying AI and ML algorithms to VLSI design, focusing on optimizing performance, reducing PPA (power, performance, area)

Course Objectives: On completion of this course, the student will be able to :

1. Understand the layout compaction, placement, and routing in VLSI design, applying design rules, compaction algorithms, circuit representation, wire length estimation, and partitioning algorithms.
2. Expertise in floor planning and routing concepts, placement algorithms, local and global routing, as well as gate-level and switch-level modeling and simulation in VLSI design.
3. Understand combinational logic synthesis, principles, implementation, and two-level logic synthesis, along with gate-level and switch-level modeling and simulation
4. Gain proficiency in high-level synthesis, covering hardware models, internal algorithm representation, allocation, assignment, scheduling algorithms, and high-level transformations in VLSI design .
5. Will explore AI's role in VLSI design, addressing advances, challenges, and applications of AI and ML algorithms to optimize performance .

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	2	2	-	-	2	-	-	-	-	-	-	-	2	2
CO2	2	2	-	2	2	-	-	-	-	-	-	-	2	2
CO3	1	2	-	2	2	-	-	-	-	-	-	-	1	2
CO4	1	1	-	3	1	-	-	-	-	-	-	-	2	3
CO5	1	2	-	3	3	-	-	-	-	-	-	-	2	2

Correlation rating: Low: 1/Medium: 2/High: 3

UNIT-I:

VLSI design automation tools- algorithms and system design, Structural and logic design, Transistor level design, Layout design, Verification methods, Design management tools.

Layout compaction, placement and routing, Design rules, symbolic layout. Applications of compaction, Formulation methods, Basic Algorithms, computational geometry Algorithms, Algorithms for constrained graph compaction, Circuit representation, Wire length estimation, Placement algorithms, partitioning algorithms.

UNIT-II:

Floor planning and routing- floor planning concepts. Shape functions and floor planning sizing. Classification of placement algorithms, recent trends, performance-based placement algorithms, Local routing, Area routing, Channel routing, global routing and its algorithms.
Simulation and logic synthesis- gate level and switch level modeling and simulation.

UNIT-III:

Introduction to combinational logic synthesis: ROBDD principles, implementation, construction and manipulation. Two level logic synthesis. Simulation and logic synthesis- gate level and switch level modeling and simulation

UNIT-IV:

High-level synthesis- hardware model for high level synthesis, Internal representation of input algorithms, Allocation, assignment and scheduling, Scheduling algorithms, Aspects of assignment, High level transformations.

UNIT-V:

Introduction to AI in VLSI design advances and challenges, Application of AI and ML algorithms to optimize the performance through finding the least cost paths, reducing PPA, optimizing cost, exploring molecular design, reducing the turn-around time through exploiting the AI strategies.

References:

1. S.H. Gerez, “Algorithms for VLSI Design Automation”, John Wiley ,1998/2013.
2. Naveed Sherwani, “Algorithms for VLSI Physical Design Automation”, (3/e), Kluwer,199

Course Code	Course Title				Core//PE/OE		
HR702EC	**CMOS ANALOG AND MIXED SIGNAL IC DESIGN**				**Core**		
Pre-requisites	**Contact Hours Per Week**				**CIE**	**SEE**	**Credits**
-	**L**	**T**	**D**	**P**			
	3	-	-	-	40	60	3

Course Objectives : The course is taught with the objectives of enabling the student to:

1. Familiarize the students with basic building blocks of Analog & Mixed signal IC design and their modeling
2. Train the students to analyze and design basic building blocks of Analog and Mixed Signal IC Design
3. Impart skills for analyzing different responses of various Amplifiers and Op-Amp, Comparator, S/H circuits etc

Course Outcomes : On completion of this course, the student will be able to :

1. Choose an appropriate model of MOSFET as per the given circuit / application /condition
2. To Analyze and Design amplifiers, Differential Amplifiers, current Mirrors for a given application/ specification
3. To Analyze the effect of frequency and noise on various building blocks of analog IC Design
4. To Analyze and Design complex analog circuits like comparator, OP-Amp and Band Gap references etc
5. Choose, Analyze and Design various switched capacitor and mixed signal circuits

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	1	1	2	1	-	-	-	-	-	-	-	-
CO2	1	2	2	3	-	-	-	-	-	-	-	-
CO3	2	2	3	3	1	-	-	-	-	-	-	-
CO4	2	2	3	3	1	-	-	-	-	-	-	-
CO5	2	1	2	3	-	-	-	-	-	-	-	-

Correlation rating: Low / Medium / High: 1 / 2 / 3 respectively

Unit-I

MOS Transistor: Structure of MOSFET, Working of MOS, Dedication of MOS IV Characteristics, Threshold Voltage of MOS, Second Order Effects; channel Length Modulation, Body Effect, sub Threshold Conduction, MOS small signal Model, MOS Capacitances, MOS Layout

Unit-II

Single Stage Amplifiers: MOS common source Amplifier, with resistive load, diode load, Current Source Load - Large Signal and Small Signal Analysis, Common Gate Amplifier, Common Drain Amplifier, Cascode Amplifier and Folded Cascode Amplifier

Current Mirrors: Simple Current Mirror, Mismatch in simple current Mirror, Cascode Current Mirror, Wide Swing Cascode Current Mirror, Wilson Current Mirror

Unit-III

Differential Amplifier: Simple MOS Differential Pair, Qualitative and Quantitative Analysis, Small Signal Analysis, Differential Amplifier with current Mirror load, Single Stage Op-Amps. Common Mode Analysis

Frequency Response: Association of Nodes with Poles, Open circuit Time Constants, Miller Theorem, Frequency response of Common Source Amplifier, CG Amplifier And CD Amplifier

Unit-IV

Two Stage Op-Amp: Slew Rate, CMRR, ICMR, Phase Margin, Design of Two Stage Op-Amp, Gain Boosting, Current Mirror Op-Amp.

Biasing Circuit: Constant Voltage References, PTAT, CTAT, Band-Gap References, Improved Band-Gap Reference Circuit

Unit-V

Sample and Hold Circuit: Working of Switch Capacitor circuits, Basic components of Switched Cap circuits, Characterization of Comparators, Static and Dynamic characteristics of Comparator Simple sample and Hold Circuits, Performance Parameters, Charge Injection Error, Modified S/H circuits.

Filters: Integrator, Parasitic insensitive switched cap integrator, delay free integrator, SFG, Filters

Suggested Reading

1. BehzadRazavi, Design of Analog CMOS Integrated Circuits, McGraw Hill Companies, 2013
2. Tony Chan Carusone, David Johns and Ken Martin, Analog Integrated Circuit Design, 2nd edition, John Wiley & sons. 2013
3. Philip E. Allen and Douglas R. Holberg, CMOS Analog Circuit Design, 2nd edition, Oxford University Press, 2010
4. Paul R. Gray, Paul J. Hurst, Stephen H. Lewis and Robert G. Meyer, Analysis and Design of Analog Integrated Circuits, 4th edition, Wiley India Private Limited, 2008

Course Code	Course Title						Core//PE/OE
HR861EC	**Project**						**Core**
Pre-requisites	**Contact Hours Per Week**				**CIE**	**SEE**	**Credits**
	L	**T**	**D**	**P**			
	-	-	-	6	50	50	3

Course Objectives

1. Prepare the student for a systematic and independent study of the state of the art topics in a broad area of VLSI Design.
2. To enhance practical and professional skills
3. To familiarize tools and techniques of systematic Literature survey and documentation

Course Outcomes : On completion of the course, students will be able to

1. To select the complex engineering problems beneficial to the industry & society and develop solutions with appropriate considerations.
2. To apply modern tools and analyze the results to provide valid conclusions.
3. To communicate effectively the solutions with report and presentation following ethics.
4. To work in teams and adapt for the advanced technological changes
5. To apply management principles to complete the project economically

CO-PO mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	3	3			2	2					
CQ2				3	3							
CO3								3		3		
CO4									3			3
CO5											3	

Note: Some of relevant COs must be mapped with the relevant PSOs based on the domain and application area of the project.

Oral presentation is an important aspect of engineering education. The objective of the course project is to prepare the student for a systematic and independent study of the state of the art topics in a broad area of VLSI design

Project topics may be chosen by the student with advice and approval from the faculty members. Students are to be assessed and evaluated as per the following criteria.

Each student is required to:

1. Submit a one-page synopsis at the beginning of the semester for display on the notice board (by 2nd week after commencement of the semester)
2. Give a 20 minutes demo and demonstrate the work through LCD power point presentation followed by a 10 minutes discussion.

3. Submit a report on the project work with list of references and slides used.

- Project reviews are to be scheduled from the 3rd week of the semester to the last week of the semester and any change in schedule should be discouraged.
- Batch size should be ONE.
- Finalization of the projects will be done by the supervisor at the concerned department.
- Two reviews to be conducted – One during 5th week and another during 10th week and final evaluation shall be conducted during 15th to 16th week.
- Students are required to give Presentations during the reviews.
- Students are required to submit project report.

Distribution of marks for Continuous Internal Evaluation (CIE) - 50 Marks

Evaluation Criteria	**Maximum Marks**
Literature Review	05
Problem Formulation	05
Design/ Methodology	15
Implementation & Results	15
Presentation & Documentation	10

Distribution of marks for Semester End Examination (SEE) – 50 Marks

Evaluation Criteria	**Maximum Marks**
Design/ Methodology	10
Implementation & Results	15
Presentation & Documentation	15
Publication in a conference/ Journal (Published / accepted)(Compulsory)	10